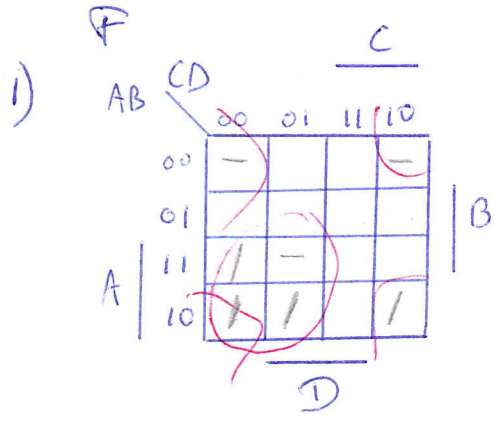


1



$$F = A \cdot \bar{C} + \bar{B} \cdot \bar{D}$$

- 2)  $\phi_1$ : Mealy  
 $\phi_2$ : 4

3) Fraction  $1.\underbrace{xxxx}_{21 \text{ bits}}x$   $\Rightarrow$  decimal value  $\geq 1$  and  $< 2$

$$q = \frac{q}{p} \times 8 \quad 2^3$$

$27 \uparrow \geq 1$

Fraction 1001  $\Rightarrow$  bit pattern 001000...0  
 Exponent  $3 + 15 = 18_{10} \Rightarrow$  bit pattern 00000 10010  
 Sign. bit 1

4)

Present state		next state		output
$F_1$	$F_0$	$\bar{X}$	$X$	
0	0	1	1	0
0	1	1	0	0
1	0	0	1	0
1	1	0	0	1

⇒

$X$	$F_1$	$F_0$	$F_1^+$	$F_0^+$	$Z$
0	0	0	1	1	0
0	0	1	1	0	0
0	1	0	0	1	0
0	1	1	0	0	1
1	0	0	0	1	0
1	0	1	1	0	0
1	1	0	1	1	0
1	1	1	0	0	1

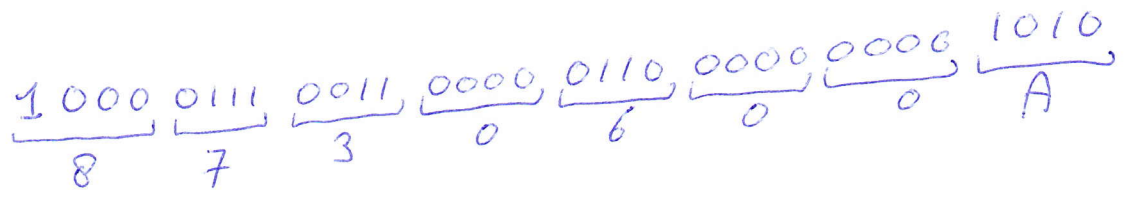
↓  
 $D_{F_1}$

$D_{F_1}$	$F_1 F_0$	$F_1$			
$X$		00	01	11	10
0		1	1	0	0
1		0	1	0	1
		$F_0$			

Q1:  $D_{F_1} = \bar{X} \cdot \bar{F}_1 + \bar{F}_1 \cdot F_0 + X \cdot F_1 \cdot \bar{F}_0$

Q2:  $Z = F_1 \cdot F_0$

5) srl %R1, 10, %R3



8 7 3 0 6 0 0 A<sub>16</sub>

6)

```

.begin
.org 0
sethi arr1, %r1
srl %r1,10,%r1      ! %r1 begin address arr1 (source)
sethi arr2, %r2
srl %r2,10,%r2      ! %r2 begin address arr2 (destination)
loop: ld[%r1], %r3    ! element of array in %r3
      addcc %r3,%r0,%r0 ! check status; result in %r0 (no change)
      be ready
      bneg skip         ! skip negative number
      st %r3, %r2       ! copy element
      addcc %r2,4,%r2   ! next address in arr2
skip: addcc %r1,4,%r1  ! next address in arr1
      ba loop
ready: st %r0, %r2     ! write terminating 0
      halt
.org 100
arr1: 12, -4, 9, 8, -23, 9, 0
.org 200
arr2:
.end

```

7) RTL of micro instruction

500: %tempϕ ← ORN (%Rϕ, %~~tempϕ~~<sup>Rϕ</sup>)  
 501: %Rϕ ← ADDCC (%tempϕ, %Rϕ)  
 502: %temp2 ← INC (%tempϕ)

	unit	after 500	after 501	after 502
%Rϕ	ϕ	ϕ	ϕ	ϕ
%tempϕ	10	1111...1 <sub>2</sub>	1111...1 <sub>2</sub>	1111...1 <sub>2</sub>
%temp1	20	20	20	20
%temp2	30	30	30	ϕ