Computer architecture and organization	Monday 13 October 2014, 8.45 – 10.30
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13 problems, 8 pages, 4 pages with the ARC docum	nentation
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Instructions for this examination.	
1. Answer the questions only in the designated	d locations on this form.
2 Fill in your name educational programme a	nd student number on the first page
2 Fill in your name at the odd pages	
5. Fin in your name at the out pages.	
4. Hand in all pages of this exam.	
5. You may only use writing material and a sim	ple calculator.
6. The documentation refers to the ARC proce	ssor. If a problem indicates that it is about the subset ARC
processor then only the instructions listed in	n figure 5-2 (documentation page 2) may be used.
, ,	
Name:	
Student number:	Educational programme:

Question 1 (2 points)

$$f(A, B, C, D) = \sum (8,9,10) + \sum_{d} (0,2,11)$$

Simplify function *f* in sum-of-products form

Question 2 (1 points)

Is the "Control Branch Logic (CBL)" in the ARC processor, see figure 5-10 (Documentation ARC, page 3), combinational logic or sequential logic?

Question 3 (1 + 1 = 2 points)



How many states does the finite state machine representation of this design have?

Is it a MEALY or a MOORE machine?

Question 4(1 + 1 = 2 points)

Given is a normalized floating point representation in base 2. The bit pattern from left to right is:

- Sign bit: 1 bit (1 is negative, 0 is positive),
- Exponent field: 5 bits in excess 10,
- Fraction field: 5 bits (not included is the hidden bit). Point is right of hidden bit.

When the exponent field is filled with all zeros, the representation is not normalized. In that case the decimal number 0 is represented, independent of the sign and fraction field.

a) What is the decimal value of bit pattern 1 01010 00000 (spaces added for readability)

b) How many representations are there for decimal 0?

Question 5 (1 points)

What is the machine code (in hexadecimal format) of the instruction:

addcc %r6, 4, %r4

Name:	
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Question 6 (1 + 2 = 3 points)

	.begin		
	.org 0		
	sethi	series,%r1	
	srl	%r1,10,%r1	! %r1 bevat nu het adres van series.
	addcc	%r0, 0, %r11	
lp:	ld	[%r1], %r10	
	addcc	%r10,%r0,%r0	
	be	rdy	
	bneg	nxt	
	addcc	%r10,%r11,%r11	
nxt:	addcc	%r1,4,%r1	
	ba	lp	
rdy:	halt		
series:	1,-6,2,-5	5,3,4,0	
	.end		

What is the content of the registers %r1 and %r11 <u>after</u> execution of this program? (Give <u>decimal</u> values).

%r1	
%r11	

Question 7 (2 + 2 = 4 points)

The state table of a synchronous state machine is:

Present state	Next	state	Output Z
	\overline{X}	X	
S0	S0	S1	0
S1	S1	S2	0
S2	S2	S3	0
S3	S3	S0	1

For the encoding of this state machine two D flip-flops are used (F1, F0) with S0=00, S1=01, S2=10 and S3=11.

Give a minimal SOP form for the data input of flip-flop F0 (i.e. DF0=f(X,F1,F0))

Give a minimal SOP form for the output Z

Question 8 (1 + 2 = 3 points)

The ARC processor is extended with the instruction MUL4. The number representation is twos complement.

```
MUL4 %rx, %rz with %rz ← 4 × %rx /* multiply with 4 */
The condition codes may change.
%rx, %ry and %rz are registers in the registerfile (%r0 until %r31).
The instruction format is:
op=10, rd=%rz, op3=?????, rs1=%rx, bit13=0, rs2 is not used
```

The decimal value of the start address of this instruction in the control memory is decimal 1784. Hint: multiplying an operand with 2 is the same as shifting the operand one position to the left.

a) What is the bit pattern of field **op3** of the instruction?

op3 =

Give an <u>efficient</u> micro-program for instruction MUL4. From the visible registers of the register file only the register indicated with %rz may change. When the instruction is finished a jump is made to address 2047 (decimal).

Use symbolic names in the fields (e.g. in field A %r6 instead of 00110). Fields that are not used must be marked with '-' (don't care). If you need more than 2 micro-instructions the maximum score for this question is 1 point.

address	А	Amux	В	Bmux	С	Cmux	Rd	Wr	ALU	Cond	Jump addr
1784											

Question 9 (3 x 1 = 3 points)

a) What is the basic principle which makes that caches are effective?

b) How many addressable words does the chip below have?



c) For which of the following two types is the data density (e.g. bits per square mm) the highest: DRAM or SRAM? Explain why.

Question 10 (1 points)

A computer system is interfaced to three devices: a printer, a disk, and a display. The characteristics of the devices are summarized in the following table.

Device	Interrupt service time	Interrupt frequency	Allowable Latency
Printer	1000 us	1/(4000 us)	2000 us
Disk	125 us	1/(1000 us)	500 us
Display	100 us	1/(1000 us)	300 us

Can the requirements given in the table above be met in case interrupts are disabled during interrupt handling? Explain why.

Name:

Question 11 (2 + 2 + 1 = 6 points)

A microcontroller has 16 address pins (A0 to A15), an 8 bit databus and uses 'memory-mapped' I/O.

Within the memory map, the following devices can be addressed with the following specifications:

ROM: 16 KBytes at the lowest addresses of the address range.

RAM: 8 KBytes directly following the address range of ROM.

Extended RAM: 32 Kbytes at the highest address range

Shadowing is not allowed.

The select lines for these areas are respectively *SelROM, SelRAM and SelExtended*. These select lines are a function of some of the address lines A0 to A15, where A15 is the most significant address line.

a) Give the **minimal** expression for *SelROM* (as a function of the address lines).

SelROM =

b) Give the **minimal** expression for *SelRam* (as a function of the address lines).

SelRAM =

c) Give the starting address of the extended RAM in hexadecimal representation

Question 12 (6 + 1 = 7 points)

A 32-bits microprocessor has an on-chip primary cache with the following characteristics:

Address space:	4 GBytes, Byte-addressing
Primary cache:	Size: 256 kBytes (excluding tags)
	Slotsize: 64 Bytes
	Organisation: Direct

a) For this primary cache, a byte-address is split into parts that are used for, respectively, comparison with the tag in the cache, selection of a slot in the cache, selection of a word in a slot and selection of a byte in a word. The cache interprets different parts of the address generated by the processor in different ways. Which address bits belong to each of these parts?



b) The data belonging to address 00000B3A Hex is in the cache. Given this information, give the range of addresses (in hexadecimal format) of which you are now sure that the data is in the cache.



Question 13 (1 point)

A number of disks, a CPU and the main memory are all connected to the same 20 MHz 16-bit bus. The disk transfer rate is 4 Mbytes/s. The CPU and main memory can both keep pace with the bus. How many disks can at maximum simultaneously be active on this bus?

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Question 1 (2 points)

$$f(A, B, C, D) = \sum (8,9,10) + \sum_{d} (0,2,11)$$

Simplify function *f* in sum-of-products form

A.!B

Question 2 (1 points)

Is the "Control Branch Logic (CBL)" in the ARC processor, see figure 5-10 (Documentation ARC, page 3), combinational logic or sequential logic?

combinational logic

Question 3 (1 + 1 = 2 points)



How many states does the finite state machine representation of this design have?



Is it a MEALY or a MOORE machine?

Mealy

Question 4(1 + 1 = 2 points)

Given is a normalized floating point representation in base 2. The bit pattern from left to right is:

- Sign bit: 1 bit (1 is negative, 0 is positive),
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When the exponent field is filled with all zeros, the representation is not normalized. In that case the decimal number 0 is represented, independent of the sign and fraction field.

a) What is the decimal value of bit pattern 1 01010 00000 (spaces added for readability)

```
Exp = 10-10=0; mantissa 1.0 \rightarrow decimal value -1
```

b) How many representations are there for decimal 0?

2^6= 64

Question 5 (1 points)

What is the machine code (in hexadecimal format) of the instruction:

addcc %r6, 4, %r4

8881A004

Name:	

Question 6 (1 + 2 = 3 points)

	.begin		
	.org 0		
	sethi	series,%r1	
	srl	%r1,10,%r1	! %r1 bevat nu het adres van series.
	addcc	%r0, 0, %r11	
lp:	ld	[%r1], %r10	
	addcc	%r10,%r0,%r0	
	be	rdy	
	bneg	nxt	
	addcc	%r10,%r11,%r11	
nxt:	addcc	%r1,4,%r1	
	ba	lp	
rdy:	halt		
series:	1,-6,2,-5	5,3,4,0	
	.end		

What is the content of the registers %r1 and %r11 <u>after</u> execution of this program? (Give <u>decimal</u> values).

%r1	68
%r11	10

Question 7 (2 + 2 = 4 points)

The state table of a synchronous state machine is:

Present state	Next	Output Z	
	\overline{X}	X	
S0	S0	S1	0
S1	S1	S2	0
S2	S2	S3	0
S3	S3	S0	1

For the encoding of this state machine two D flip-flops are used (F1, F0) with S0=00, S1=01, S2=10 and S3=11.

Give a minimal SOP form for the data input of flip-flop F0 (i.e. DF0=f(X,F1,F0))

DF1=X.!F0 +X . !F0

Give a minimal SOP form for the output Z

Z= F1.F0

Question 8 (1 + 2 = 3 points)

The ARC processor is extended with the instruction MUL4. The number representation is twos complement.

```
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The decimal value of the start address of this instruction in the control memory is decimal 1784. Hint: multiplying an operand with 2 is the same as shifting the operand one position to the left.

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op3 = 1111110

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Use symbolic names in the fields (e.g. in field A %r6 instead of 00110). Fields that are not used must be marked with '-' (don't care). If you need more than 2 micro-instructions the maximum score for this question is 1 point.

address	А	Amux	В	Bmux	С	Cmux	Rd	Wr	ALU	Cond	Jump addr
1784	_	1	_	_	_	1	0	0	lshif t2	Jmp	2047

Question 9 (3 x 1 = 3 points)

a) What is the basic principle which makes that caches are effective?

```
Principle of locality of reference
Only a small portion of data/code is used within a certain period of time.
```

b) How many addressable words does the chip below have?

1K or 1024.

		\cup		
A0 A1 A2 A3 A4 A5 CS, CE CDD	1 2 3 4 5 6 7 8		18 17 16 15 14 13 12 11	 VCC A9 A8 A7 D4 D3 D2 D1 WE
GILD	,		10	

c) For which of the following two types is the data density (e.g. bits per square mm) the highest: DRAM or SRAM? Explain why.

DRAM. One SRAM cell consists of 6 transistors and one DRAM cell of 1 transistors and a capacitor.

Name:

Question 10 (1 points)

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Can the requirements given in the table above be met in case interrupts are disabled during interrupt handling? Explain why.

No, Diring interrupt handling of the printer, the disk and display cannot be dealt with.

Question 11 (2 + 2 + 1 = 6 points)

A microcontroller has 16 address pins (A0 to A15), an 8 bit databus and uses 'memory-mapped' I/O.

Within the memory map, the following devices can be addressed with the following specifications:

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The select lines for these areas are respectively *SelROM, SelRAM and SelExtended*. These select lines are a function of some of the address lines A0 to A15, where A15 is the most significant address line.

a) Give the **minimal** expression for *SelROM* (as a function of the address lines).

```
SelROM = !A15&!A14
```

b) Give the **minimal** expression for *SelRam* (as a function of the address lines).

```
SelRAM = !15 & A14 & !A13
```

c) Give the starting address of the extended RAM in hexadecimal representation

8000Hex

Name:

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32 bits => 1 punt Voor elk vak aantal bits goed => 4x1 punt Adresnummering goed => 1 punt

b) The data belonging to address 00000B3A Hex is in the cache. Given this information, give the range of addresses (in hexadecimal format) of which you are now sure that the data is in the cache.



Question 13 (1 point)

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 $20*10^{6}$ words/s on the bus = $40*10^{6}$ bytes/s Disks generate 4 Mbytes/s => 40/4 = 10 disks can be active simultaneously