

Pearls of Computer Science (201700139)

Pearl 000: Binary logic and computer architecture

September 6, 2019 test

Answers

1. Binary Numbers

4 pt (a) F.

4 pt (b) B.

4 pt (c) F.

4 pt (d) G.

4 pt (e) G.

4 pt (f) E.

The rule in answer E takes care of the fact that both 1111 and 0000 represent the number zero. So when a carry happens (i.e., when the addition crosses the 1111 \rightarrow 0000 boundary), we need to increment the result by 1 extra.

For example, suppose we have -2 and add 3 to it. That's $1101 + 0011 = (1)0000$, where the (1) is the carry bit. Obviously, $-2 + 3 = +1$, but 0000 represents 0. By incrementing the number by one when the carry is set, 0000 will be changed to 0001, representing $+1$, as needed.

(Since it was a multiple-choice question, just finding the answer by trying a few examples was enough; we didn't ask for a complete proof.)

2. Boolean logic

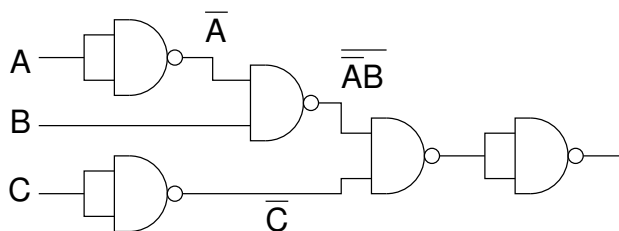
4 pt (a) A, A, B, A

8 pt (b) E, D, D, -, B, F

As announced during the exam, question MC14 should be skipped. Accidentally, I made two changes at this point, one of which is correct ($\overline{Y} + Y = 1$, the complement rule) and the other (involving the last factor) is wrong. Of course, this means the whole step is wrong (answer F), but since it is confusing we removed this question.

6 pt (c) Using DeMorgan: $\overline{(\overline{A} \cdot B) + C} = \overline{(\overline{A} \cdot B)} \cdot \overline{C}$

This leads to the following circuit:



There are also other possibilities.

4 pt (d) C and F are both correct.

The 4-input NAND should output a 0 only if all four inputs are 1.

The first 2 NANDs will each output a 0 when both their inputs are 1; so we need to connect their outputs to something that gives a 0 iff both inputs are 0: that's an OR gate (answer C).

Alternatively, by putting inverters after the first two NAND-gates, we change them into AND-gates; AND'ing their outputs makes a 4-input AND, and inverting that (in the final NAND-gate) gives a 4-input NAND (answer F).

4 pt (e) A.

3. Problem 3

	read address 1 / write address	read address 2	instruction
Timeslot 0	2	1	1
Timeslot 1	3	1	1
Timeslot 2	1	2	0
Timeslot 3	1	3	0
Timeslot 4			

4. Problem 4

18 pt

(a)

R17	R18	R19	R20
4			
	8		
		6	
			8
		-2	
		8	
			4
		0	
			0

BREQ not taken

BRNE taken to sub r19,r18

BREQ taken, skips 1 instruction

BRNE not taken

5 pt

(b) 15 since 13 instructions are executed, two of which are a branch that is taken and thus take 1 extra cycle each.

5. Problem 5

$$f(X, Y) = X + (X+1) + \dots + (Y-1) = \sum_{k=X}^{Y-1} k = \frac{Y \cdot (Y-1)}{2} - \frac{X \cdot (X-1)}{2}$$

Each pass through the loop adds R17 to R19, and increments R17 by 1; R17 initially is X, so we add first X, then X+1, then X+2, and so on into R19. We stop when R17 has reached the value of R18, i.e., Y.

Full score already for the $X + (X + 1) + \dots + (Y - 1)$ answer.