Computer architecture and organization Diagnostic test

3 problems, 4 pages

Instructions for this examination:

1. Answer the questions only in the designated locations on this form.
2. Fill in your name, educational programme and student number on the first page.
3. Fill in your name at the odd pages.
4. Hand in all pages of this exam.
5. You may only use writing material and a simple calculator.
6. The documentation refers to the ARC processor. If a problem indicates that it is about the **subset ARC** processor then only the instructions listed in figure 5-2 (documentation page 2) may be used.

Name: .....
Student number: ..... Educational programme: .....

QUESTION 1: **(2 X 1 = 2 POINTS)**

Answer the following questions

a) Is a DRAM in general bigger or smaller than an SRAM cell? Why?

b) Which type of memory needs to be refreshed? Why?

QUESTION 2: **(4 + 1 + 4 = 10 POINTS)**

A 32-bit microprocessor contains an on-chip primary cache and an off-chip secundary cache with the following specifications:

Addressspace:	8 GB, Byte-addressing
Primary cache:	Size: 64 kB (excluding tags)
	Slotsize: 128 B
	Organisation: 8-voudig set-associative
Secundary cache:	Size: 512 kB (excluding tags)
	Slotsize: 32 B
	Organisation: direct

The next question deals with the **primary cache**.

a) For the primary cache, the byte-address is split into parts that are used for comparison with respectively the tag in the cache, the selection of a slot in the cache, the selection of a word in a slot and the selection of a byte in a word. Which bitnumbers belong to each of the parts?

The following questions deal with the secondary cache. This cache consists of a separate tag and data part.

b) How many data-words does the secondary cache have?

c) For the secondary cache the byte-address is split into parts that are used for comparison with respectively the tag in the cache, the selection of a slot in the cache, the selection of a word in a slot and the selection of a byte in a word. Which bitnumbers belong to each of the parts?

Naam: ……..

QUESTION 3 **(4 × 1 = 12 POINTS)**

An ‘embedded’ microcontroller is used for controlling a heating system. The microcontroller has 10 address pins (A0 until A9), an 8 bit data bus and makes use of ‘I/O-mapped’ I/O. For the selecting the memory space, the M/In is asserted (made high), for selecting the I/O space, M/In is deactivated (made low). The memory system consists of ROM and RAM according the following specifications:

ROM: 256 Bytes at the lowest addresses of the address range
RAM: 128 Bytes at the highest addresses of the address range.
Shadowing is allowed.

Within the I/O space, burners and water pumps are addressed according the following specifications:

Burners 128 Bytes at the lowest addresses of the address range.
Water pumps: 128 Bytes directly following the address range for the burners.
Because of safety reasons, shadowing is not allowed within the I/O space

The select lines for these areas are respectively *SelROM, SelRAM, SelBurn* and *SelWater*. These select lines are a function of a selection of address lines and the signal M/In.

a) Give the minimal logical expression for *SelROM* (as a function of the address lines and M/In).

b) Give the minimal logical expression for *SelRAM* (as a function of the address lines and M/In).

c) Give the minimal logical expression for *SelBurn* (as a function of the address lines and M/In).

d) Give the minimal logical expression for *SelWater* (as a function of the address lines and M/In).

QUESTION 4 **(2 POINTS)**

A computer system is interfaced to three devices: a printer, a disk, and a display. The characteristics of the devices are summarized in the following table.

Device	***Interrupt service time***	***Interrupt frequency***
Printer	1000 us	1/(4000 us)
Disk	125 us	1/(1000 us)
Display	100 us	1/(1000 us)

A program P, which performs only computation (no input/output), takes 100 s to run when no input/output is being performed.

How long will it take for P to run when all of the above devices are operating at their maximum speeds?